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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/626,366	LIM ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8,11-13,15-17,19 and 20* is/are rejected.

7)☒ Claim(s) *7,9,10 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because the reference numerals and the lead lines in Fig. 1A-2, 4 and 5 are not clear and legible.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Election/Restriction

2. Applicant's election with traverse of Group I, claims 1-13 in Paper No. 3 is acknowledged. The grouping of the claims 1-20 as shown in the restriction requirement in paper no. 2, dated 05-30-04, inadvertently included the following:

I. Group I (device claims): Claims 1-13

II. Group II (method claims): Claims 14-20

The correction in the restriction requirement includes the following groups/claims:

I. Group I: Claims 1-13 and 15-20, drawn to a semiconductor device, classified in class 257, subclass 691.

II. Group II: Claim 14, drawn to a method of making a semiconductor device, classified in class 438, subclass 106.

Therefore, previous grouping of the device claims (paper no. 2) has been withdrawn and the corrected grouping including the device claims 1-13 and 15-20 of group I have been incorporated in the examination in the office action set forth below.

3. Applicant's election with traverse of the device claims in Paper No. 2 is acknowledged. The traversal is on the ground(s) that in the requirement for an election, Groups I (device claims 1-13 and 15-20) and II (method claim 14) differ only in a semiconductor device and method for making the same. Requiring an election based on the above-noted differences would appear to be unwarrant since the fields of search

appear to be almost identical. This is not found persuasive because referring to the restriction requirement set forth in the Office Action paper no.2, it clearly shows that the alternative method proposed by the examiner would be distinct from the process claimed. Additionally, the search is not coextensive as evidenced by the different fields of search for the process and product as cited in the previous restriction requirement. Furthermore, Applicant has not provided a convincing argument that the materially different processes would not be suitable in producing the claimed device.

The requirement is still deemed proper and is therefore made FINAL.

Claim Objections

4. Claim 10 is objected to because of the following informalities:

A. The limitations as recited in line1, include " the first ring segments of the first power ring are larger than the second ring segments of the second power ring".

It is not clear from the claim language if the segments are larger in a number of segments or a dimension such as length, width, spacing between the segments, etc.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

6. Claims 1-5,11-13, 15, 16, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (APA) in view of Chu et al. (US Pat. 5801440).

Regarding claims 1-5, 12 and 13, the APA (Fig. 1A/1B) discloses a ball grid array (BGA) package comprising:

- a substrate (100 in Fig. 1A/1B) having a front side and a back side
- a die attachment region (see Fig. 1A/1B)formed on the front side of the substrate
- an electrically conductive first power ring (110 in Fig. 1B) formed on the front side of the substrate, the first ring being arranged around the die attachment region
- an electrically conductive second power ring (120 in Fig. 1B) on the front side of the substrate, the second ring segments being arranged around the die

attachment region and positioned at a greater distance from the die attachment region than the first power ring

- a third conductive ring arranged around the die attachment region and positioned at a closer distance to the die attachment region than the first and second power rings, the third conductive ring being a ground ring
- a plurality of vias (141-144 in Fig. 1A/1B) penetrating through the substrate, including: a subgroup of first vias which are connected to the first power ring; and a subgroup of second vias which are connected to the second power ring (see 142 and 143 respectively in Fig. 1A/1B)
- a semiconductor die (160 in Fig. 1A/1B) mounted over the die attachment region on the front side of the substrate, the semiconductor chip having a plurality of bond pads (161, 162, etc. in Fig. 1A/1B), and
- bonding wires (171, 172, etc. in Fig. 1A/1B) for connecting the plurality of bond pads of the die to associated first, second and third rings

(Fig. 1A/1B; specification pages 1-4).

APA fails to teach the first, second and third rings including a plurality of spaced apart ring segments such that the segments of the first/second power rings and ground ring comprise separate/independent power source and grounding respectively.

APA (Fig. 2) teaches a conventional configuration of wiring where a second power rings includes a plurality of spaced apart ring segments comprising four separate/independent power sources (see 231-234 in Fig. 2; specification pages 2-4) to provide the desired number of different power/voltages.

Chu et al. teach a BGA substrate (10 in Fig. 1-5) having a configuration of ground ring and power rings where a second power ring is segmented into a plurality of segments (see 26, 28, 30, 32, etc. in Fig. 2), each segment being connected to respective one, two or more vias (see 78, 90, etc. in Fig. 2 and 3) and solder balls to provide the desired separate/independent power/voltages to achieve the desired signal to power/ground contact ratio, via spacing and the conductive trace routing (Col. 4, line 16-51; Col. 2-4).

Furthermore, determination of parameters such as number of bonding segments/traces, vias/contacts in respective power, ground or signal wiring, dimension of conductive trace including thickness/width, spacing/pitch of the vias/solder balls, etc. is a subject of routine experimentation and optimization in chip packaging and interconnect technology to achieve the desired electrical functionality, signal/noise ratio, grounding requirements.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the plurality of spaced apart ring segments such that the segments of the first/second power rings and ground ring comprise

separate/independent power source and grounding respectively as taught by APA and Chu et al. so that the desired signal/noise ratio and grounding requirements can be achieved and the routing/wiring layout and electrical performance can be improved in the APA's BGA package.

Regarding claim 11, APA and Chu et al. teach substantially the entire claimed structure as applied to claim 1 above, wherein the APA teaches a plurality of solder balls formed on the back side of the substrate where the solder balls being electrically connected to the respective vias, but fail to teach an encapsulation layer which protectively encases the front side of the substrate encasing at least a portion of the semiconductor die and the bonding wires.

Chu et al. teach conventional BGA packages having an encapsulation layer protectively encasing a front side of the substrate encasing at least a portion of the semiconductor die and the bonding wires to provide the desired surface protection (Col. 1, lines 15-32).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the encapsulation layer which protectively encases the front side of the substrate encasing at least a portion of the semiconductor die and the bonding wires as taught by Chu et al. so that the surface protection can be improved in Chu et al. and APA's BGA package.

Regarding claims 15, 16 and 19, APA and Chu et al. teach substantially the entire claimed structure as applied to claims 1-5 above.

Regarding claim 20, APA and Chu et al. teach substantially the entire claimed structure as applied to claims 1 and 11 above.

7. Claims 6, 8 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the APA and Chu et al. (US Pat. 5801440) as applied to claims 1 and 15 above, and further in view of Currie et al. (US Pat. 5530287).

Regarding claims 6, 8 and 17, APA and Chu et al. teach substantially the entire claimed structure as applied to claim 1 above, except the plurality of spaced apart first ring segments are arranged in staggered configuration relative to those of the second ring.

Currie et al. teach a bonding pattern/configuration in a substrate (30/38 in Fig. 6), the substrate having conductive tabs/segments in a plurality of rows/rings (see 20-1, 20-2, etc. in rows 1, 2, etc. in Fig. 6 where the pattern has a staggered arrangement to provide the dimensional flexibility for the conductor/wiring and improved reliability (Col. 5, line 5- Col. 6, line 5).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate except the plurality of spaced apart first ring segments are arranged in staggered configuration relative to those of the second ring

and the first ring segments and each of the first ring segments is connected to at least two of the first vias as taught by Currie et al. so that the desired wiring dimensions can be selected and the spacing/wiring layout can be improved in Chu et al. and APA's BGA package.

Allowable Subject Matter

8. Claims 7, 9 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for Allowance

9. The following is an examiner's statement of reasons for allowance:

The references of record do not teach either singularly or in combination at least the limitations " each of the first ring segments includes a conductive tab that electrically connects the first ring segments to at least some of the first vias; and wherein the conductive tabs of the first ring segments are arranged so that they pass through spaces between the plurality of spaced apart conductive second ring segments" in a BGA substrate having a ground ring and segmented first and second power rings where the plurality of segments are spaced apart and arranged in a staggered configuration.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

Nitin Parekh

PATENT EAMINER

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07-16-04